

CLAIMS:

1. A device (30) applicable for non-volatile memory purposes or latch-up circuits, the device comprising:
 - a selection device (22) having a control electrode (13) and a first dielectric layer insulating the control electrode from the rest of the selection device, and
 - 5 - a storage device (23) comprising a second dielectric layer, wherein the first dielectric layer of the selection device (22) and the second dielectric layer of the storage device (23) are individual parts of one and the same ferroelectric layer (14).
- 10 2. A device according to claim 1, wherein the selection device is a transistor (22) comprising a gate electrode (13), a gate dielectric and a drain (19) and a source (20) and wherein the storage device is a capacitor (23) comprising a first electrode (12), a dielectric layer and a second electrode (18), wherein the gate dielectric of the transistor (22) and the dielectric layer of the capacitor (23) are individual parts of one and the same ferroelectric layer (14).
- 15 3. The device (30) according to claim 1, wherein the gate electrode (13) of the transistor (22) and the first electrode (12) of the capacitor (23) are individual parts of a first conductive layer.
- 20 4. The device (30) according to any of the previous claims, wherein the drain (19) and source (20) of the transistor (22) and the second electrode (18) of the capacitor (23) are individual parts of a second conductive layer.
- 25 5. The device (30) according to claim 1, wherein one of the first (12) and second (18) electrode of the capacitor (23) is electrically connected to drain (19), the source (20) or the gate (13) of the transistor (22).

6. The device (30) according to claim 1, wherein the gate electrode (13), the drain (19) and the source (20) of the transistor (22) and the first electrode (12) and the second electrode (18) of the capacitor (23) are formed of PEDOT/PSS.

5 7. The device (30) according to claim 1, the device (30) furthermore comprising a semiconductive layer (21).

8. The device (30) according to claim 7, wherein the semiconductive layer (21) is an organic semiconductive layer.

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9. The device (30) according to claim 1, wherein the ferroelectric layer (14) comprises a hole (16).

10. A method for processing device (30) applicable for non-volatile memory
15 purposes or latch-up circuits comprising a selection device (22) comprising a control electrode (13), a first dielectric layer and a first (19) and second (20) main electrode, and a storage device (23) comprising a first electrode (12), a second dielectric layer and a second electrode (18), the method comprising:
- providing and patterning of a first conductive layer onto a substrate (10), thus
20 forming the first electrode (12) of the storage device (23) and the control electrode (13) of the selection device (22),
- providing and patterning of a ferroelectric layer (14) on the patterned first conductive layer, thus forming the first dielectric layer of the selection device (22) and the second dielectric layer of the storage device (23), and
25 - providing and patterning of a second conductive layer on the patterned ferroelectric layer (14), thus forming the second electrode (18) of the capacitor (23) and the first (19) and second (20) main electrode of the selection device (22).

11. The method according to claim 10, wherein providing of the ferroelectric layer
30 (14) is providing of a ferroelectric polymer layer.

12. The method according to claim 10, wherein patterning the ferroelectric layer (14) comprises crosslinking the ferroelectric layer.